IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants	:	Merwin H. Alferness et al.
Serial No.	:	10/667,029
Filed	:	September 18, 2003
For	:	METHODS AND APPARATUS FOR ALLOCATING BANDWIDTH FOR A NETWORK PROCESSOR
Examiner	:	Tanh Q Nguyen
Group Art Unit	:	2182
Confirmation No.	:	9131
Customer No.	:	46628

Mail Stop Appeal Brief-Patents
Commissioner for Patents
P.O. Box 1450
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APPELLANTS' BRIEF - REPLACEMENT SECTION

Dear Sir:

In response to the Notification of Non-Compliant Appeal Brief, Appellants respectfully submit the following replacement section.

SUMMARY OF CLAIMED SUBJECT MATTER

CLAIM 1

Independent claim 1 is directed to a method of self-adjusting allocation of memory bandwidth in a network processor system. The method comprises determining an amount of memory bandwidth of a network processor used by a plurality of data types to transmit data through a plurality of active ports (e.g., as discussed on page 10, lines 26-31 of the specification). The method further comprises determining an amount of memory bandwidth of the network processor used by each of the plurality of data types (e.g., as discussed on page 10, lines 3-6 of the specification). The method further comprises dynamically adjusting an amount of memory bandwidth allocated to at least one of the plurality of data types based on the determinations (e.g., as discussed on page 8, lines 10-14 and pages 11-12, lines 28- of the specification (e.g., “activating a port” based on “C-limit - A-rate - E-rate”).

CLAIM 12

Independent claim 12 is directed to an apparatus. The apparatus comprises port activation logic adapted to couple to a memory of a network processor (e.g., 114 and 104 of FIG. 1 and as discussed on pages 4-5, lines 31-27). The port activation logic is further adapted to interact with the memory so as to determine an amount of memory bandwidth of the network processor used by a plurality of data types to transmit data through a plurality of active ports (e.g., as discussed on page 10, lines 26-31 of the specification). The port activation logic is

further adapted to interact with the memory so as to determine an amount of memory bandwidth of the network processor used by each of the plurality of data types (e.g., as discussed on page 10, lines 3-6 of the specification). The port activation logic is further adapted to interact with the memory so as to dynamically adjust an amount of memory bandwidth allocated to at least one of the plurality of data types based on the determinations (e.g., as discussed on page 8, lines 10-14 and pages 11-12, lines 28-8 of the specification).

CLAIM 23

Independent claim 23 is directed to a network processor system. The network processor system comprises a memory (e.g., 104 of FIG. 1 and as discussed on pages 4-5, lines 19-27 of the specification). The network processor system further comprises a network processor coupled to the memory (e.g., 102 of FIG. 1 and as discussed on pages 4-5, lines 19-27 of the specification). The network processor comprises a memory controller (e.g., 108 of FIG. 1 and as discussed on pages 4-5, lines 19-27 of the specification). The network processor further comprises a plurality of ports (e.g., 106, 112 of FIG. 1 and as discussed on pages 4-5, lines 19-27 of the specification). The network processor further comprises port activation logic coupled to the memory controller and the plurality of ports and the memory (e.g., 114 of FIG. 1 and as discussed on pages 4-5, lines 19-27 of the specification). The port activation logic is adapted to interact with the memory so as to determine an amount of memory bandwidth of the network processor used by a plurality of data types to transmit data through a plurality of active ports (e.g., as discussed on page

10, lines 26-31 of the specification). The port activation logic is further adapted to interact with the memory so as to determine an amount of memory bandwidth of the network processor used by each of the plurality of data types (e.g., as discussed on page 10, lines 3-6 of the specification). The port activation logic is further adapted to interact with the memory so as to dynamically adjust an amount of memory bandwidth allocated to at least one of the plurality of data types based on the determinations (e.g., as discussed on page 8, lines 10-14 and pages 11-12, lines 28-8 of the specification).

"MEANS" OR "STEP"

None of the claims contain an element expressed as a means or step for performing a specified function without the recital of structure, material, or acts in support thereof.